HyperTransport™ (HT) Technology Physicals

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Physical Design Objectives

- **Very simple to engineer in system**
- **Wide range of performance**
  - 1.6Gbits/s to 102Gbits/s
- **Low pin count Chip to Chip interconnect**
  - On-board, board-board, short cable
- **Hot-Plug for system fault resilience**
  - Requires HT Switch

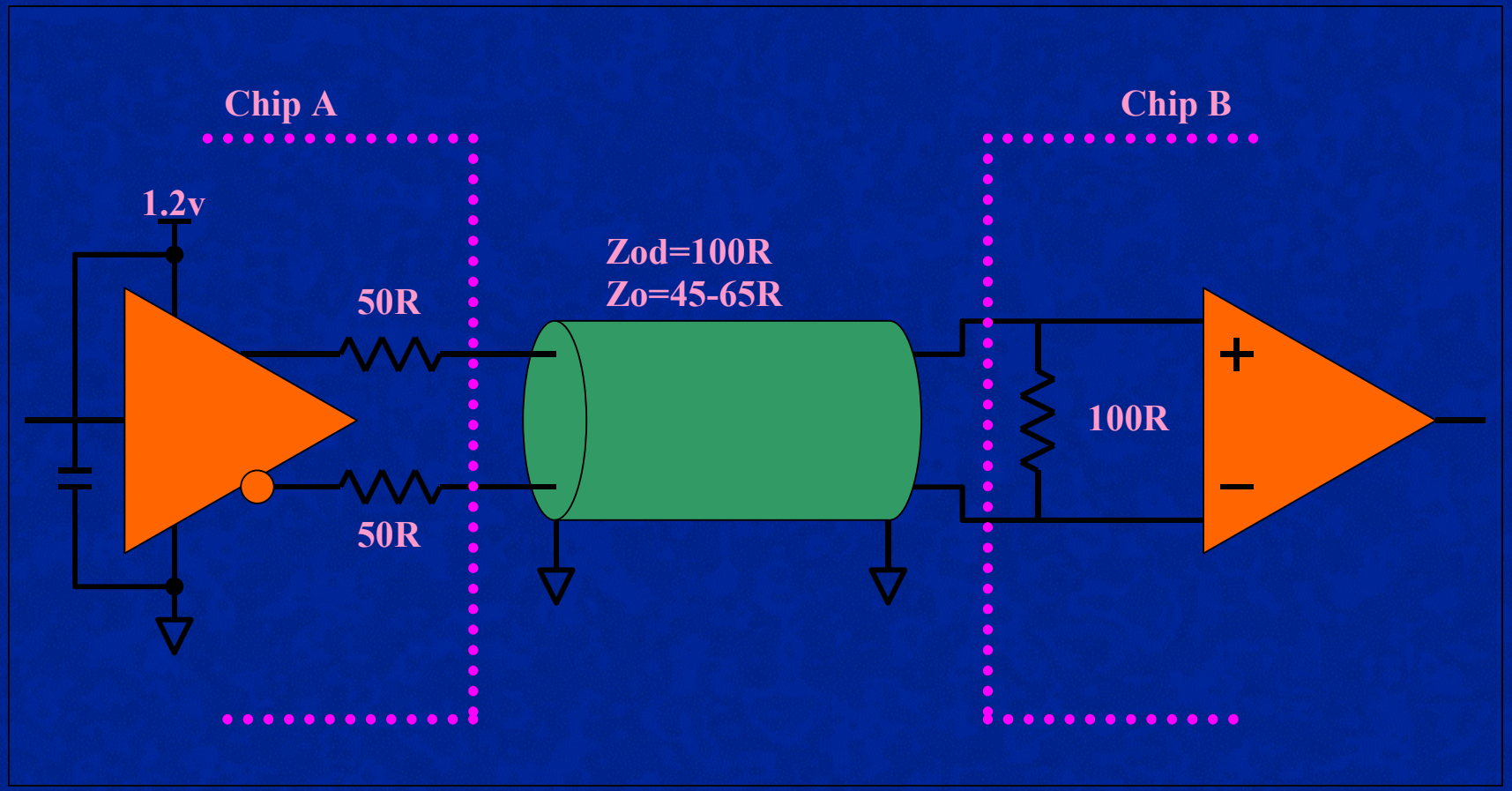
Physical Interconnect

- **Point-point, uni-directional signaling**
  - Link is bi-directional, so two sets of wires
- **Differential, 600mV voltage swing**
  - Voltage levels derived from 1.2v supply
- **On-chip, double ended termination**
  - Receiver and transmitter match interconnect impedance
- **Quadrature clock with data DDR**
  - Data width 2, 4, 8, 16, 32 bits plus 1 control bit
  - One clock for up to 8 bits of data

Scalable bandwidth

- **HT supports a set of six fixed transfer rates**
  - 400MT/s to 1.6GT/s
  - A device's minimum requirement is to support 400MT/s
- **HT supports datapath widths 2 to 32 bits**
  - Wider devices must support narrower interfaces
- **Protocol supports a discovery phase after reset**
  - Links starts up at 400MT/s
  - Hardware configures link for 2, 4, 8 bits
  - Configuration software programs CSR's for operational data rate and width

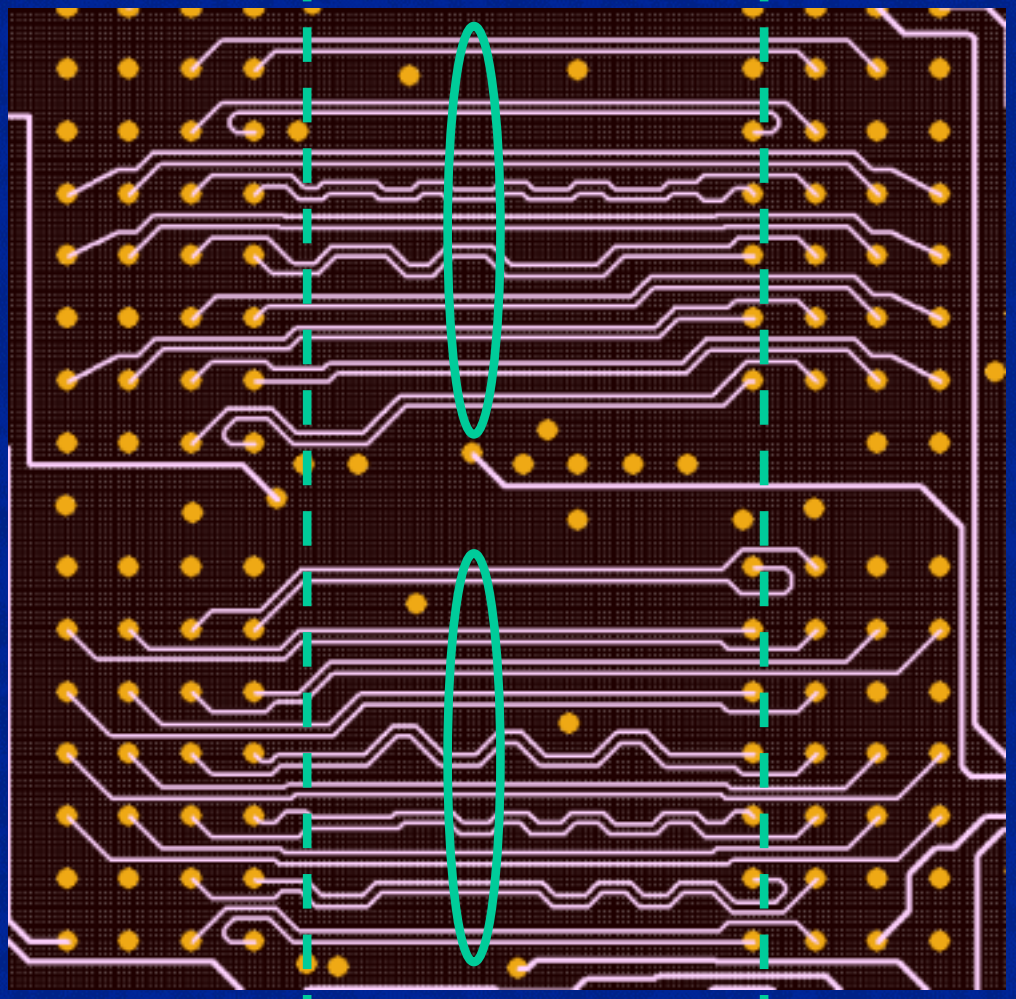
Idealized Transmitter and Receiver



Board design considerations

- **All traces routed at same length**
  - Tx Quadrature clock avoids delaying clock in etch or Rx
- **On-chip termination avoids PCB stubs**
  - Saves significant board area and difficult to place components
- **On-chip decoupling for 1.2v HT supply rail**
  - Tx terminates common and differential mode reflections
- **On-chip calibration for driver and receiver termination**
  - External resistors set termination value

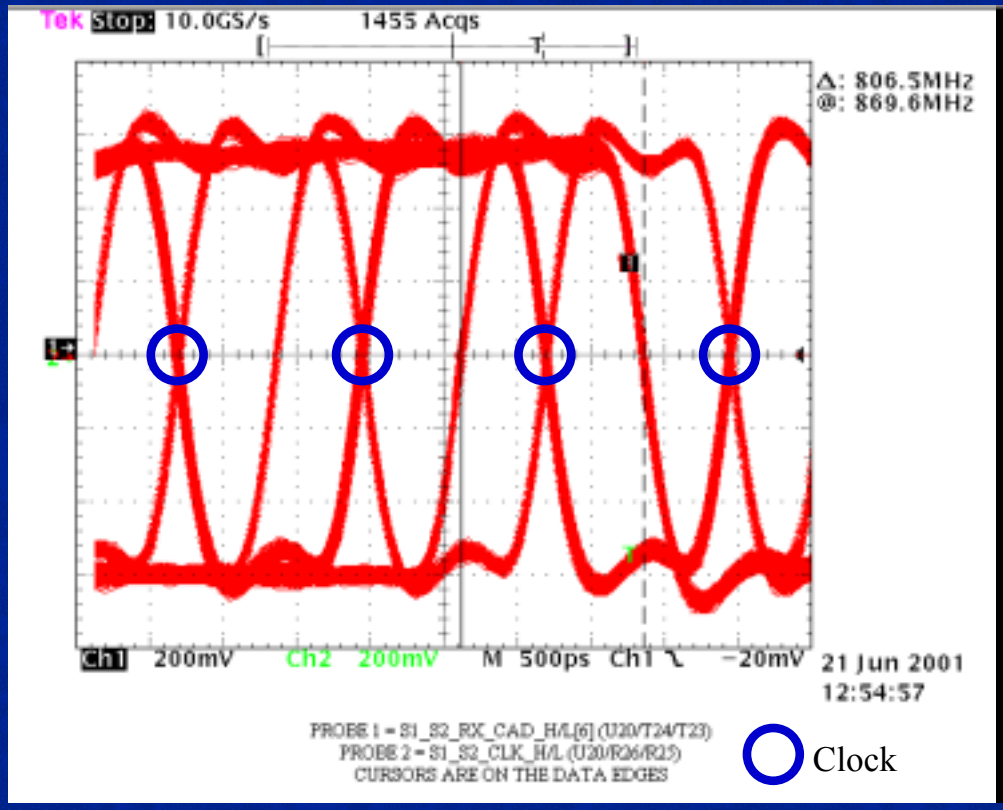
HT Routing example

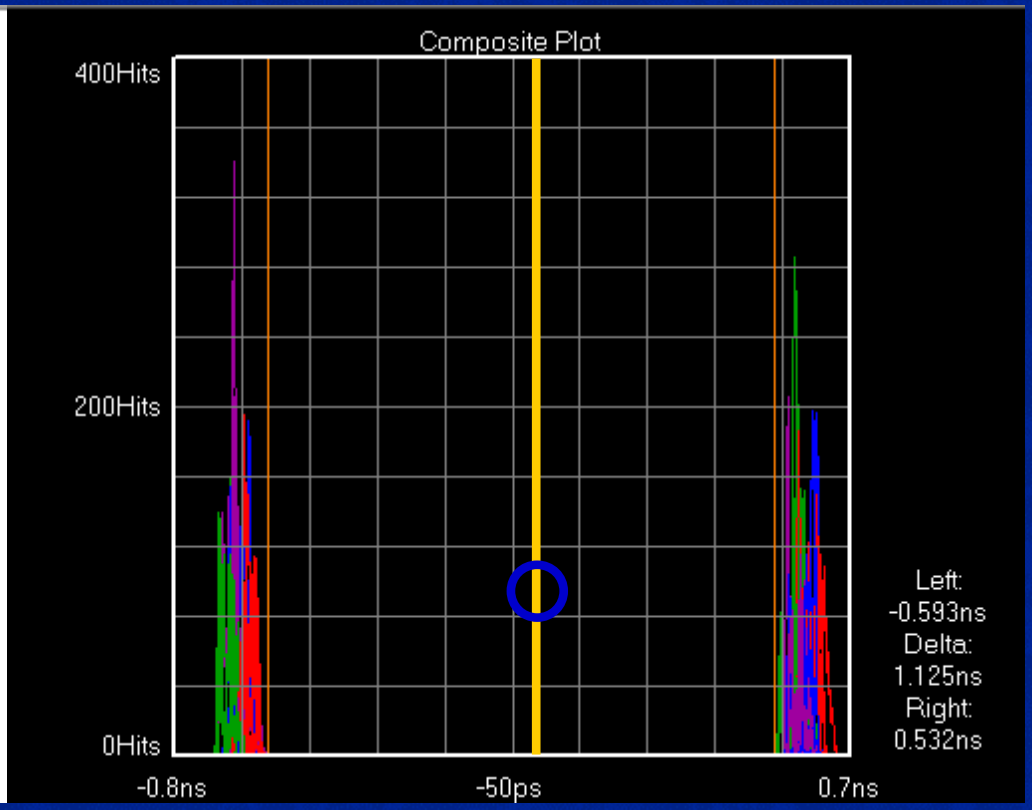


Chip A 8 bit link Chip B

- 8 bit HT link between two AP1011s
- Each pair within an 8 bit group is matched to within 25pS
- Pairs are routed as 3.75mil line, 5 mil space
- Zod=100ohm
  Zo=52ohm
- Maximum etch length is 24-30 inches depending on stack-up

HT measurements on PCB





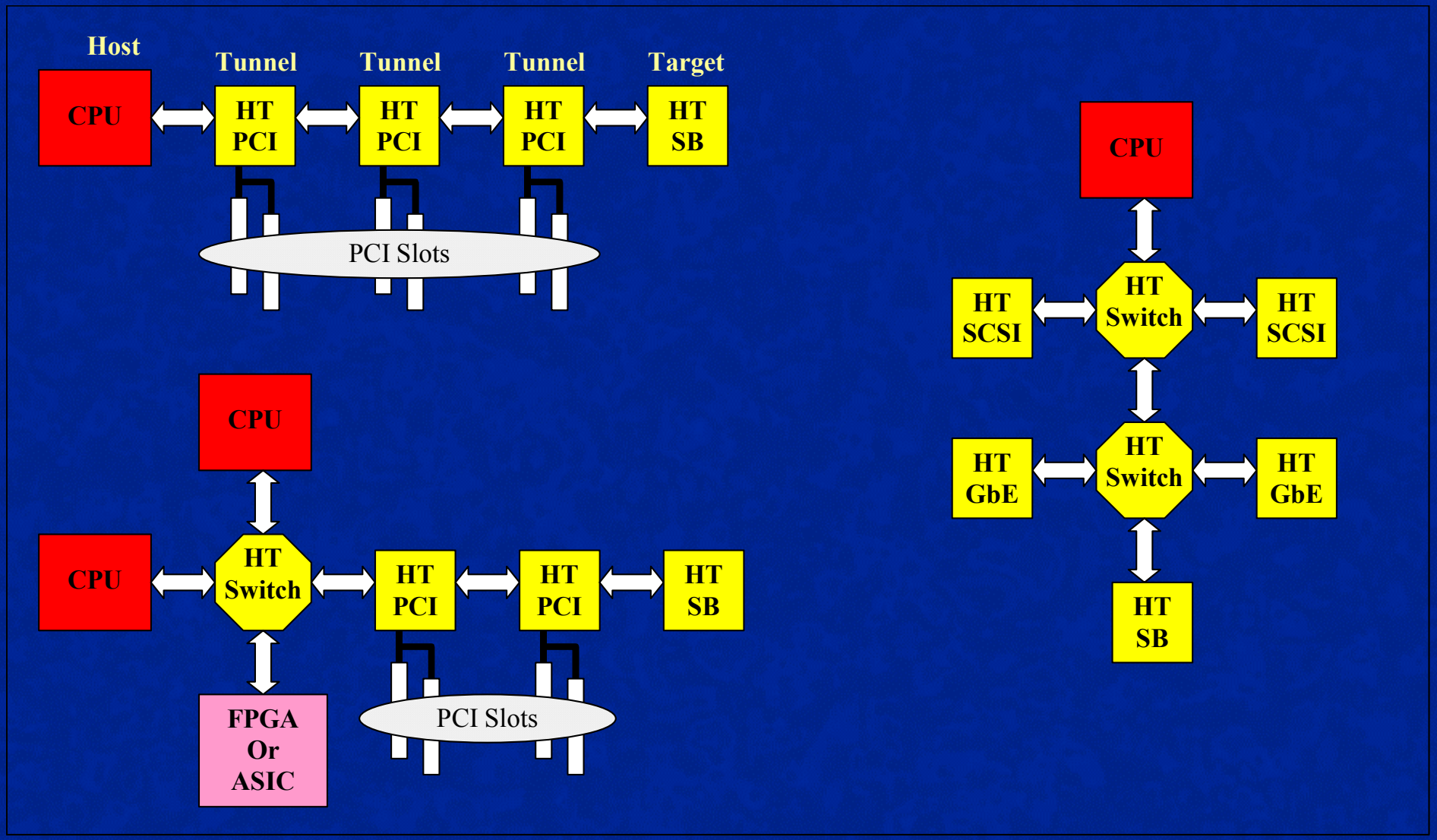
AP1011 HT-PCI Bridge
Data eye relative to clock
Measured at receiver @ 800Mbit/sec

AP1011 HT-PCI Bridge
Data eye relative to clock all bits all edges
Data is valid 0.59nS before and 0.53nS after clock
Measured at receiver @ 800Mbit/sec or +/-0.625nS

Topologies

- **There are three types of HT devices**
  - Host
    - Primary attachment to CPU or Switch
  - Tunnel
    - Slave device that can be daisy-chained
  - Target
    - Slave device at end point of an LDT chain
- **Slave devices can be bridges or controllers**
  - E.g. HT-PCI, HT-GbE
- **Switches allow chains to be connected**
  - Switch ports can be either Host or Slave

Example Topologies



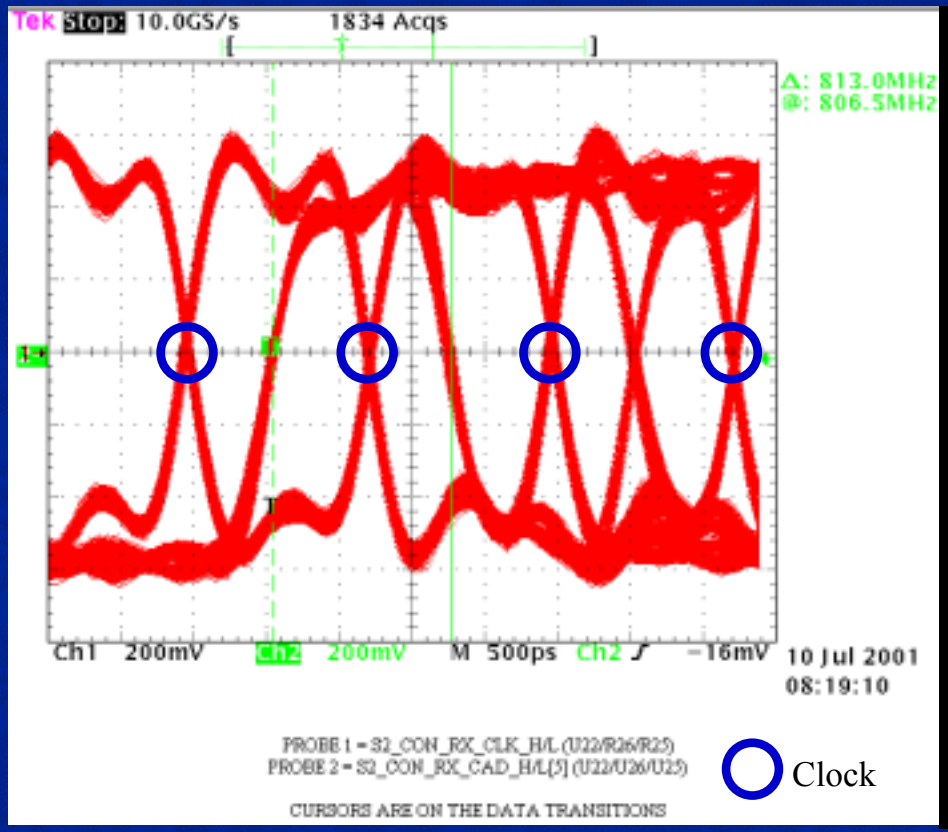
Future HT developments

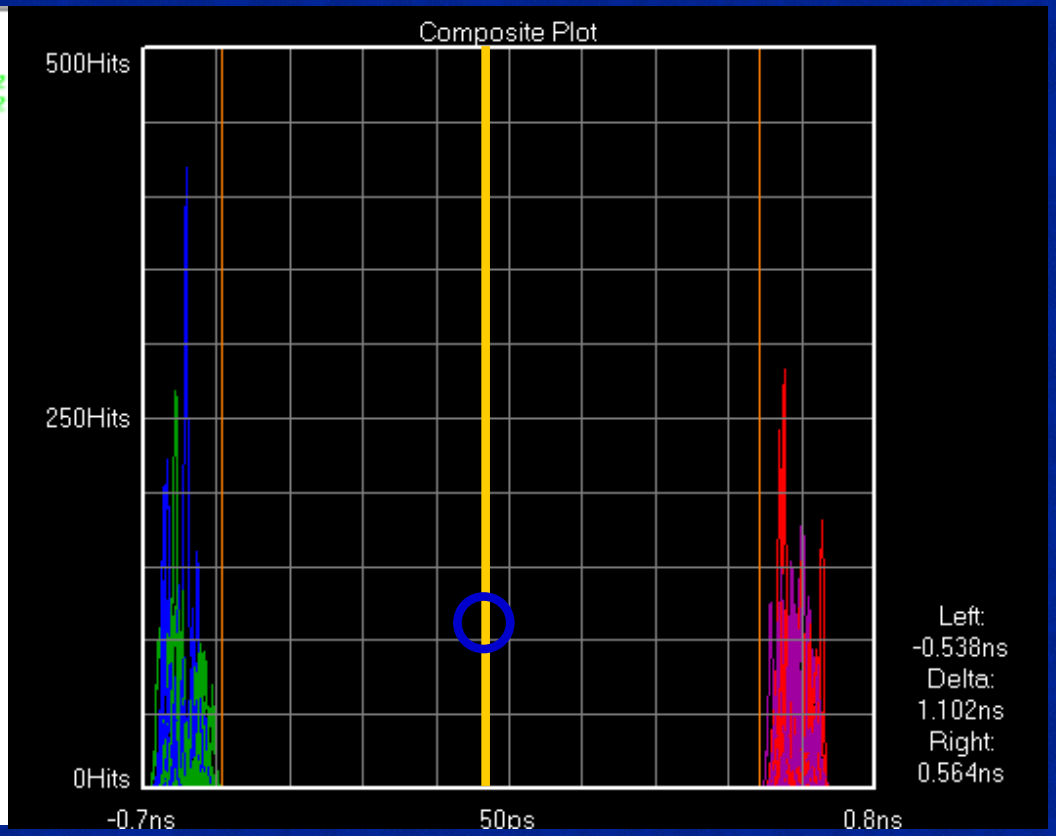
- **HT is a "short distance" interconnect**
  - Initially chip-to-chip on a board up to 30 inches
- **HT signaling capability**
  - Motherboard to daughter card
  - Backplane applications
  - Cabling solutions within a box
  - Short cables between adjacent boxes

HT through connectors

- **HT's differential signaling can be used through connectors and short cables**
  - Limiting factors are interconnect loss and skew
  - Common mode offsets between the signaling devices
- **HT switches enable HT backplane systems**
  - Including hot-plug
- **Cable lengths of up to 6 feet are feasible at 800MT/s (see technology demo in booth #17)**
  - Sufficient to allow compute and I/O to be in separate boxes
  - Allows for incremental I/O expansion

HT measurements through 6 feet of cable





AP1011 HT-PCI Bridge through 6' cable
Data eye relative to clock
Measured at receiver @ 800Mbit/sec

AP1011 HT-PCI Bridge through 6' cable
Data eye relative to clock all bits all edges
Data is valid 0.53nS before and 0.56nS after clock
Measured at receiver @ 800Mbit/sec or +/-0.625nS

HT Hot-Plug

- **Switches support hot-plug**
  - SHPC compatible
  - Can be used for board-board, board-backplane, board-cable systems
- **Switch has a pin per port that is asserted during hot-plug sequence**
  - Tristates that port's HT I/O's
  - Terminates and flushes all outstanding transactions to/from the port
  - Software reconfigures devices on port after completion of hot-plug sequence

Conclusions

- HT provides a simple reliable system level method of connecting devices at high speed
- By supporting a range of transfer rates and bit widths a wide range of system configurations are possible
- With the use of a HT switch more complex I/O architectures are possible
- Board to board connectors and cabling can be used to increase system architecture flexibility
- HT switches support “hot-plug” for systems with fault resilience requirements